

## CLAIMS

What is claimed is:

- 5 1. A two-dimensional array of processing elements wherein:  
each processing element in the interior of the array comprises:  
two inputs from processing elements on either side along a first dimension of the array;  
two outputs to processing elements on either side along a second dimension of the array; and  
Boolean logic circuitry for generating an output signal that is a Boolean function of two  
10 input signals ;  
and at least some of the processing elements in the interior of the array comprise:  
circuitry for changing the magnitude of the output signal from the Boolean logic circuitry  
and for applying it to both outputs; and  
threshold circuitry for comparing signals on the two inputs with a threshold value and  
15 providing binary input signals to the Boolean logic circuitry having a first value if the signal on an  
input exceeds the threshold and a second value if the signal on the input does not exceed the  
threshold value; and  
some processing elements on the edge of the array comprise:  
a first input from a processing element in the interior of the array;  
20 a second input from outside of the array;  
two outputs to processing elements on either side along the edge of the array;  
a differential amplifier for comparing signals on the first and second inputs and providing  
a binary output signal having a first value if the signal on the second input exceeds the signal on the  
first input and a second value if the signal on the second input does not exceed the signal on the first  
25 input; and  
circuitry for changing the magnitude of the binary output signal and for applying it to both  
outputs.
2. An analog-to-digital converter comprising:  
30 an analog signal input  
a two-dimensional array of interconnected processing elements having a plurality of  
attractors each known to be associated with at least one digital value wherein:  
each processing element in the interior of the array comprises:  
two inputs from processing elements on either side along a first dimension of the array;  
35 two outputs to processing elements on either side along a second dimension of the array; and

Boolean logic circuitry for generating an output signal that is a Boolean function of two input signals ;

and at least some of the processing elements in the interior of the array comprise:

circuitry for changing the magnitude of the output signal from the Boolean logic circuitry

5 and for applying it to both outputs; and

threshold circuitry for comparing signals on the two inputs with a threshold value and providing binary input signals to the Boolean logic circuitry having a first value if the signal on an input exceeds the threshold and a second value if the signal on the input does not exceed the threshold value; and

10 some processing elements on the edge of the array comprise:

a first input from a processing element in the interior of the array;

a second input connected to the analog signal input;

two outputs to processing elements on either side along the edge of the array;

a differential amplifier for comparing signals on the first and second inputs and providing

15 a binary output signal having a first value if the signal on the second input exceeds the signal on the first input and a second value if the signal on the second input does not exceed the signal on the first input; and

circuitry for changing the magnitude of the binary output signal and for applying it to both outputs;

20 means for detecting into which attractor the array of interconnected processing elements has fallen.

3. An analog-to-digital converter comprising:

an analog signal input;

25 a plurality of two-dimensional arrays of interconnected processing elements each having at least one attractor known to be associated with at least one digital value wherein:

each processing element in the interior of the array comprises:

two inputs from processing elements on either side along a first dimension of the array;

two outputs to processing elements on either side along a second dimension of the array; and

30 Boolean logic circuitry for generating an output signal that is a Boolean function of two input signals ;

and at least some of the processing elements in the interior of the array comprise:

circuitry for changing the magnitude of the output signal from the Boolean logic circuitry

and for applying it to both outputs; and

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threshold circuitry for comparing signals on the two inputs with a threshold value and providing binary input signals to the Boolean logic circuitry having a first value if the signal on an input exceeds the threshold and a second value if the signal on the input does not exceed the threshold value; and

- 5       some processing elements on the edge of the array comprise:  
a first input from a processing element in the interior of the array;  
a second input connected to the analog signal input;  
two outputs to processing elements on either side along the edge of the array;  
a differential amplifier for comparing signals on the first and second inputs and providing  
10 a binary output signal having a first value if the signal on the second input exceeds the signal on the first input and a second value if the signal on the second input does not exceed the signal on the first input; and

circuitry for changing the magnitude of the binary output signal and for applying it to both outputs;

- 15       means for detecting into which attractor each array of interconnected processing elements has fallen, and for generating an output signal identifying the digital value(s) known to be associated with that attractor; and

a voting circuit for identifying the digital value identified the most number of times in the output signals from the plurality of arrays.

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4. A signal processor comprising:

a signal input;

a two-dimensional array of interconnected processing elements having a plurality of attractors each known to be associated with an output value wherein;

- 25       each processing element in the interior of the array comprises:  
two inputs from processing elements on either side along a first dimension of the array;  
two outputs to processing elements on either side along a second dimension of the array; and  
Boolean logic circuitry for generating an output signal that is a Boolean function of two input signals ;

- 30       and at least some of the processing elements in the interior of the array comprise:  
circuitry for changing the magnitude of the output signal from the Boolean logic circuitry and for applying it to both outputs; and

threshold circuitry for comparing signals on the two inputs with a threshold value and providing binary input signals to the Boolean logic circuitry having a first value if the signal on an

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input exceeds the threshold and a second value if the signal on the input does not exceed the threshold value; and

some processing elements on the edge of the array comprise:  
a first input from a processing element in the interior of the array;  
5 a second input connected to the signal input;  
two outputs to processing elements on either side along the edge of the array;  
a differential amplifier for comparing signals on the first and second inputs and providing  
a binary output signal having a first value if the signal on the second input exceeds the signal on the  
first input and a second value if the signal on the second input does not exceed the signal on the first  
10 input; and  
circuitry for changing the magnitude of the binary output signal and for applying it to both  
outputs; and  
means for detecting into which attractor each array of interconnected processing  
elements has fallen.

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5. A signal processor comprising:  
a signal input;  
a plurality of two-dimensional arrays of interconnected processing elements each  
having at least one attractor known to be associated with an output value wherein;  
20 each processing element in the interior of the array comprises:  
two inputs from processing elements on either side along a first dimension of the array;  
two outputs to processing elements on either side along a second dimension of the array; and  
Boolean logic circuitry for generating an output signal that is a Boolean function of two  
input signals ;  
25 and at least some of the processing elements in the interior of the array comprise:  
circuitry for changing the magnitude of the output signal from the Boolean logic circuitry  
and for applying it to both outputs; and  
threshold circuitry for comparing signals on the two inputs with a threshold value and  
providing binary input signals to the Boolean logic circuitry having a first value if the signal on an  
30 input exceeds the threshold and a second value if the signal on the input does not exceed the  
threshold value; and

some processing elements on the edge of the array comprise:  
a first input from a processing element in the interior of the array;  
a second input connected to the signal input;  
35 two outputs to processing elements on either side along the edge of the array;

a differential amplifier for comparing signals on the first and second inputs and providing a binary output signal having a first value if the signal on the second input exceeds the signal on the first input and a second value if the signal on the second input does not exceed the signal on the first input; and

5       circuitry for changing the magnitude of the binary output signal and for applying it to both outputs; and

means for detecting into which attractor each array of interconnected processing elements has fallen; and for generating an output signal identifying the output value; and

a voting circuit for identifying the output value identified the most number of times  
10 in the output signals from the plurality of arrays.

6.       A method of operating a two-dimensional array of interconnected processing elements having a plurality of attractors each known to be associated with at least one digital value  
15 wherein:

each processing element in the interior of the array comprises:

two inputs from processing elements on either side along a first dimension of the array;

two outputs to processing elements on either side along a second dimension of the array; and

Boolean logic circuitry for generating an output signal that is a Boolean function of two  
20 input signals ;

and at least some of the processing elements in the interior of the array comprise:

circuitry for changing the magnitude of the output signal from the Boolean logic circuitry and for applying it to both outputs; and

threshold circuitry for comparing signals on the two inputs with a threshold value and  
25 providing binary input signals to the Boolean logic circuitry having a first value if the signal on an input exceeds the threshold and a second value if the signal on the input does not exceed the threshold value; and

some processing elements on the edge of the array comprise:

a first input from a processing element in the interior of the array;

30 a second input from outside of the array;

two outputs to processing elements on either side along the edge of the array;

a differential amplifier for comparing signals on the first and second inputs and providing a binary output signal having a first value if the signal on the second input exceeds the signal on the first input and a second value if the signal on the second input does not exceed the signal on the first  
35 input; and

circuitry for changing the magnitude of the binary output signal and for applying it to both outputs,

said method comprising the steps of:

- 5           applying an input signal to at least one second input; and
- detecting into which attractor the array has fallen.

7.       The method of claim 6 comprising the step of applying the input signal in parallel to a plurality of second inputs.

- 10       8.       The method of claim 6 comprising the steps of:
  - applying the input signal in parallel to second inputs in a plurality of arrays of interconnected processing elements having a plurality of attractors each known to be associated with at least one digital value; and
  - identifying the output value associated the most number of times with the attractors
- 15       into which the arrays have fallen.

9.       The method of claim 6 wherein the input signal is an analog signal and the output signal is a digital signal.

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10.      A method of operating a plurality of two-dimensional arrays of interconnected processing elements each having at least one attractor known to be associated with at least one output value wherein:

- 25           each processing element in the interior of the array comprises:
  - two inputs from processing elements on either side along a first dimension of the array;
  - two outputs to processing elements on either side along a second dimension of the array; and
  - Boolean logic circuitry for generating an output signal that is a Boolean function of two input signals ;

30           and at least some of the processing elements in the interior of the array comprise:

- circuitry for changing the magnitude of the output signal from the Boolean logic circuitry and for applying it to both outputs; and

          threshold circuitry for comparing signals on the two inputs with a threshold value and providing binary input signals to the Boolean logic circuitry having a first value if the signal on an input exceeds the threshold and a second value if the signal on the input does not exceed the

35 threshold value; and

- some processing elements on the edge of the array comprise:  
a first input from a processing element in the interior of the array;  
a second input from outside of the array;  
two outputs to processing elements on either side along the edge of the array;
- 5 a differential amplifier for comparing signals on the first and second inputs and providing  
a binary output signal having a first value if the signal on the second input exceeds the signal on the  
first input and a second value if the signal on the second input does not exceed the signal on the first  
input; and  
circuitry for changing the magnitude of the binary output signal and for applying it to both
- 10 outputs,
- said method comprising the steps of:
- applying an input signal in parallel to at least one second input in each array; and  
detecting into which attractor each array has fallen.
- 15 11. The method of claim 10 comprising the step of applying the input signal in parallel  
to a plurality of second inputs in each array.
12. The method of claim 10 comprising the step of:  
identifying the output value associated the most number of times with the attractors
- 20 into which the arrays have fallen.
13. A method of developing a signal filter comprising:  
creating a first number of agents, each agent characterized by a predetermined number of  
adjustable parameters corresponding to at least one type of signal, each of said parameters having
- 25 a range of possible values;  
establishing constraints for adjusting said adjustable parameters;  
adjusting the parameters of each of said agents in accordance with at least one predetermined  
rule until reaching a predetermined criterion.

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